Patent Claims

1. A circuit for addressing a memory (1), to which input data (Din) can be written at different write addresses (Wa) with a first clock rate (Wclk) and from which output data (RAM_Do) can be read at different read addresses (Ra) with a second clock rate (Rclk), it being possible for the memory to be fed a write reset pulse (Wres) that resets the write address to an initial value, and it being possible for the memory to be fed a read reset pulse (Rres) that resets the read address to an initial value, wherein switching means (6, 7, 8, 9) are provided in order to derive the read reset pulse from the write reset pulse.

2. The circuit as claimed in claim 1, wherein the circuit comprises a detector (2) set up in order to detect synchronization data from the input data in order to generate the write reset pulse.

3. The circuit as claimed in claim 1, wherein the circuit comprises an adjustable delay element (14) having a fixed temporal relationship of the read-out data (Dout) with regard to a read-side start pulse (SyncR).

4. The circuit as claimed in claim 3, wherein the circuit has a counter (12) that is started by the start pulse and counts down proceeding from a start value as far as an end value.

5. The circuit as claimed in claim 4, wherein the circuit is provided with a storage means (13), in which the present value (Count) of the counter (12) is stored if a read-side reset pulse (Rres) occurs.

6. The circuit as claimed in claim 5, wherein a connection is provided between the storage means and the adjustable delay element, said connection being set up in order to write the stored value of the counter (Delay) as a delay value to the adjustable delay element.

7. The circuit as claimed in claim 1, wherein switching means (6, 7, 8, 9) are provided in order to detect from the write-side reset pulse (Wres) a pulse edge that triggers the generation of a read-side reset pulse (Rres).

8. The circuit as claimed in claim 1, wherein provision is made of counters (4, 11) that generate the write and read address, respectively, of the memory (1).

9. The circuit as claimed in claim 8, wherein the counters are clocked with the write and read clock signal, respectively.